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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/910,447	07/19/2001	Toshihiko Higuchi	81754.0064	2754

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EXAMINER
LE, THAO X

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 11/13/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/910,447	Applicant(s) HIGUCHI, TOSHIHIKO	
	Examiner Thao X Le	Art Unit 2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) *13-20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12 and 21-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

2. Claims 1-4, 7, 8, 10, 12 and 32 are rejected under 35 U.S.C. 102(e) as being anticipated by US 6201278 to Gardner et al.

Regarding to claim 1, Gardner discloses a semiconductor device in fig. 5A-5K comprising: a semiconductor substrate 502, column 12 line 62, a gate electrode 530, column 13 line 66, formed on the semiconductor substrate through a gate dielectric layer 524, first and second impurity diffusion layers 508A and 508B, column 13 line 49, formed in the semiconductor substrate and opposed to each other with the gate electrode being interposed between them, a third impurity diffusion layer 552, fig. 5E, column 13 line 21, formed in a portion immediately below the gate electrode in the semiconductor substrate, and a sidewall dielectric layer 522A and 522B, column 13 line 38, formed on the side surface section of the gate electrode, wherein the gate electrode has a width that gradually increases from a bottom thereof toward an upper surface thereof, and wherein surfaces of the first and second impurity diffusion layers are located at a position higher than an interface between the semiconductor substrate and the gate dielectric layer, fig. 5K.

Regarding to claim 2, Gardner discloses the semiconductor device wherein a distance between the surface of the first and second impurity diffusion layers and the interface between the semiconductor substrate and the gate dielectric between about 0.20 μm, column 3 line 10 (channel length).

Regarding to claim 3, Gardner discloses a semiconductor device wherein the groove section 514, column 13 line 11, is formed at a specified location in the semiconductor substrate, and the gate electrode 530 is formed on a bottom surface of the groove section through the gate dielectric layer 524, fig 5a-5K.

Regarding to claims 4, 7, 8, 10, 12 Gardner discloses a semiconductor device wherein the gate electrode 530 may be formed by depositing the conductive material or semiconductor material, at least one alloy that includes at least two constituents selected from polycrystalline silicon, tungsten, tantalum, copper and gold, column 13 line 66 and column 14 line 61, wherein the first and second impurity diffusion layers include an extension 552A/552B, fig. 5K, wherein the a third impurity diffusion layer 552, fig. 5E is formed in a portion immediately below the gate electrode in the semiconductor substrate, wherein the sidewall dielectric layer 522A/522B is formed from a material including silicon oxide, column 13 line 38, wherein the sidewall dielectric layer 522A/522B has an outer surface that is generally vertical with respect to the surface of the semiconductor substrate, and film thickness that gradually reduces from a bottom thereof toward an upper surface thereof, fig. 5K.

Regarding to claim 32, Gardner discloses a semiconductor device in fig. 5A-5K comprising: a semiconductor substrate 502, column 12 line 62, a groove section 514, fig. 5D, formed at a specified location in the semiconductor substrate, a gate electrode 530, column 13

line 66, formed on a bottom surface of the groove section through a gate dielectric layer 524, wherein the gate electrode has a width that gradually increases from a bottom thereof toward an upper surface thereof, and a width of the upper surface of the gate electrode substantially equals to a width of the groove, fig. 5K.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 5-6, 9, 11 and 21-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 6201278 to Gardner et al in view of US 6214679 to Murthy et al.

Regarding to claims 5-6, 25-26, Gardner does not expressly disclose the semiconductor device wherein an element isolation region or STI is formed in the semiconductor substrate and dielectric layer embedded therein.

But Murthy reference discloses the semiconductor device wherein an element isolation region 204. fig. 12 is formed in the semiconductor substrate and dielectric layer embedded therein. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use STI teaching of Murthy with Gardner's device, because such STI is well known in the art. Such STI can be further found in Gardner (US 6130454), Tseng (US 2001/0045608), etc...

Regarding to claims 9, 29 Gardner does not expressly disclose the semiconductor device wherein the metal silicide layer is formed on the first and second impurity diffusion layers, and the gate electrode includes a metal silicide layer on an upper surface thereof.

But Murthy reference discloses the semiconductor device wherein the metal silicide layer 236 is formed on the first and second impurity diffusion layers 218, and the gate electrode 206 includes a metal silicide layer 236, fig. 12, on an upper surface thereof. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use silicide layer teaching of Murthy with Gardner, because it would have reduced the resistance of polysilicon as taught by Murthy, column 1 line 47-48.

Regarding to claim 11, Gardner does not expressly disclose the semiconductor device wherein the surface of the first and second impurity diffusion layers are formed at a position higher than a surface of the STI.

But Murthy reference discloses the semiconductor device in fig. 12 wherein the surface of the first and second impurity diffusion layers 218 are formed at a position higher than a surface of the STI. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use the elevated source and drain teaching of Murthy with Gardner's device, because it would have increased the conductivity and good punch through characteristics obtained as taught by Murthy, column 5 line 62-67.

Regarding to claim 21, Gardner discloses a semiconductor device in fig. 5A-5K comprising: a semiconductor substrate 502, column 12 line 62, a gate electrode 530, column 13 line 66, formed on the semiconductor substrate through a gate dielectric layer 524, first and

second impurity diffusion layers 508A and 508B, column 13 line 49, formed in the semiconductor substrate and opposed to each other with the gate electrode being interposed between them, a sidewall dielectric layer 522A and 522B, column 13 line 38, formed on the side surface section of the gate electrode, wherein the gate electrode has a width that gradually increases from a bottom thereof toward an upper surface thereof, and wherein surfaces of the first and second impurity diffusion layers are located at a position higher than an interface between the semiconductor substrate and the gate dielectric layer, fig. 5K.

But Gardner does not expressly disclose the semiconductor device wherein surfaces of the surface of the first and second impurity diffusion layers are formed at a position higher than a surface of the STI.

But Murthy reference discloses the semiconductor device in fig. 12 wherein the surface of the first and second impurity diffusion layers 218 are formed at a position higher than a surface of the STI. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use the elevated source and drain teaching of Murthy with Gardner's device, because it would have increased the conductivity and good punch through characteristics obtained as taught by Murthy, column 5 line 62-67.

Regarding to claim 22-24, 27-28, 30-31 Gardner discloses the semiconductor device wherein a distance between the surface of the first and second impurity diffusion layers and the interface between the semiconductor substrate and the gate dielectric between about 0.20 μm, column 3 line 10 (channel length), wherein the groove section 514, column 13 line 11, is formed at a specified location in the semiconductor substrate, and the gate electrode 530 is formed on a bottom surface of the groove section through the gate dielectric layer 524, fig 5a-5K, wherein the

gate electrode 530 may be formed by depositing the conductive material or semiconductor material, at least one alloy that includes at least two constituents selected from polycrystalline silicon, tungsten, tantalum, copper and gold, column 13 line 66 and column 14 line 61, wherein the first and second impurity diffusion layers include an extension 552A/552B, fig. 5K, wherein the a third impurity diffusion layer 552, fig. 5E is formed in a portion immediately below the gate electrode in the semiconductor substrate, wherein the sidewall dielectric layer 522A/522B is formed from a material including silicon oxide, column 13 line 38, wherein the sidewall dielectric layer 522A/522B has an outer surface that is generally vertical with respect to the surface of the semiconductor substrate, and film thickness that gradually reduces from a bottom thereof toward an upper surface thereof, fig. 5K.

Response to Arguments

5. Applicant's arguments with respect to claims 1-12 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thao X Le whose telephone number is 703-306-0208. The examiner can normally be reached on M-F from 8:00 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M Fahmy can be reached on 703-308-4918. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Thao X. Le
November 4, 2002

PHAT X. CAO
PRIMARY EXAMINER